IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): D.B. Kramer et al.
Case: 7-20
Serial No.: 10/085,219
Filing Date: February 28, 2002
Group: 2616
Examiner: Rhonda L. Murphy

Title: Processor With Dynamic Table-Based Scheduling Using Linked Transmission Elements For Handling Transmission Request Collisions

---

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter "Appellants" hereby appeal the final rejection dated February 5, 2008 of claims 1-10 and 18-22 of the above-identified application. A Notice of Appeal is submitted concurrently herewith.

Because prosecution was reopened by the Examiner prior to a decision on the merits by the Board of Patent Appeals and Interferences, the fee paid with the prior Notice of Appeal and Appeal Brief dated April 30, 2007 should be applied to the present Notice of Appeal and Appeal Brief. See MPEP §§ 1207.04 and 1208.02; see also 35 U.S.C. §134(a) (emphasis added) ("An applicant for a patent, any of whose claims has been twice rejected, may appeal from the decision of the primary examiner to the Board of Patent Appeals and Interferences, having once paid the fee for such appeal.")

REAL PARTY IN INTEREST

The present application is assigned of record to Agere Systems Inc. On April 2, 2007, the assignee Agere Systems Inc. completed a merger with LSI Logic Corporation, with the resulting entity being named LSI Corporation. LSI Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on February 28, 2002 with claims 1-22. Claims 1-22 remain pending. Claims 1, 11, 16, 17, 21 and 22 are the independent claims. Claims 11-17 are allowed.

Each of claims 1-10 and 18-22 stands rejected under 35 U.S.C. §103(a). Claims 1-10 and 18-22 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor that comprises scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements and traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements. The scheduling circuitry is configured for utilization of at least one time slot table comprising a plurality of locations, each corresponding to a transmission time slot and being configured to store at least one entry. The scheduling circuitry is operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time

slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

In an illustrative embodiment, shown in FIG. 3 of the drawings and described in the specification at, for example, page 6, line 1, to page 8, line 22, and page 16, lines 13-22, processor 102 comprises scheduler 306 for scheduling data blocks for transmission from a plurality of transmission elements (e.g., those associated with transmit queue 302) and traffic shaping engine 304 coupled to scheduler 306 and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements. Scheduler 306 is configured for utilization of at least one time slot table 308 comprising a plurality of locations, each corresponding to a transmission time slot and being configured to store at least one entry. As discussed in the specification, with reference to FIG. 7 of the drawings, at, for example, page 14, line 9 to page 16, line 12, scheduler 306 is operative in conjunction with time slot table 308 to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by traffic shaping engine 304 in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

Independent claim 21 is a directed to a method for use in a processor for scheduling data blocks for transmission from a plurality of transmission elements. The method comprises a step of establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements. The method further comprises a step of scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more transmission time slots. This step utilizes at least one time slot table comprising a plurality of locations, each of which corresponds to one of the transmission time slots and is configured to store at least one entry. The step may further utilize a linking of colliding transmission elements and movement of at least one entry from a first location within the at least one time slot table to a

second location within the at least one time slot table. An illustrative technique is provided in the specification, with reference to FIG. 7 of the drawings, at, for example, page 14, line 9 to page 16, line 12, wherein the traffic shaping requirement is a desired order of transmission.

Independent claim 22 is directed to a computer-readable medium comprising one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements, utilizing at least one time slot table comprising a plurality of locations, each of which corresponds to a transmission time slot and is configured to store at least one entry. The one or more programs when executed, implements a step of establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements. It further implements a step of scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more of the transmission time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

In the illustrative embodiments described in the specification at, for example, page 5, lines 1-28, the computer-readable medium may be, for example, internal memory 104 and/or external memory 106, as shown in FIGS. 1 and 2. This computer-readable medium comprises one or more programs which, when executed on processor 102 as shown in FIGS. 1 and 2, implements the illustrative technique described in the specification, with reference to FIG. 7 of the drawings, at, for example, page 14, line 9 to page 16, line 12, wherein the traffic shaping requirement is a desired order of transmission.

The claimed invention provides a number of significant advantages over conventional arrangements. See the specification at, for example, page 3, lines 25-27 ("Advantageously, the techniques of the invention can accommodate multiple simultaneous collisions of transmission requests, and greatly facilitate the provision of QoS, CoS or other desired service levels for network connections.") and at page 4, lines 26-29 ("The present invention in an illustrative embodiment improves scheduling operations in a network processor or other processor through the use of a table-based scheduling technique which allows multiple transmission elements to be

assigned to the same transmission time slot, while also maintaining a desired traffic shaping for the transmitted data blocks.")

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-10 and 18-22 stand rejected under 35 U.S.C. §103(a) over Patent No. 5,712,851 (hereinafter "Nguyen") in view of U.S. Patent No. 6,477,168 (hereinafter "Delp").

ARGUMENT

Appellants respectfully submit that the Nguyen and Delp references fail to teach or suggest the limitations of independent claim 1. For example, claim 1 recites "moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table." An illustrative embodiment of an arrangement falling with this limitation is described in the present specification at, for example, page 13, lines 21-23 ("Once FP and AP have separated, every time AP encounters a valid element in a time slot, then that element is written to the location pointed to by FP, deleted from the location pointed to by AP, and both FP and AP are incremented by one time slot.") and page 14, lines 22-24 ("[I]t is apparent from the foregoing example that transmission elements may move within the time slot table. As described above, this occurs when AP has separated from FP and AP encounters a valid element in its corresponding time slot.") See also FIG. 7, which shows element Q5 in the sixth time slot of the exemplary time slot table at T=5 and in the fourth slot of the exemplary time slot table at T=6.

On page 4, fourth paragraph, of the present Office Action, the Examiner concedes that Nguyen fails to disclose moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table. However, on page 4, fifth paragraph, of the present Office Action, the Examiner contends that block 708 of FIG. 7 of Delp discloses moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

Appellants respectfully disagree. Block 708 of FIG. 7 of Delp is labeled "MOVE CURRENT TIME SLOT FORWARD 1 TIME SLOT 708," and described in Delp at column 7, lines 11-15:

> When the current time slot is empty, then the current time is compared with the current time slot as indicated at a decision block 706. If the current time is greater than the current time slot, then the current time slot is moved forward one time slot as indicated at a block 708.

Moving a current time slot forward does not entail moving an entry from one location within a time slot table to another location, but rather merely indicates incrementing a variable. See Delp at column 5, lines 54-56, and at column 6, lines 4-12 (emphasis added):

> Cell/frame scheduler 102 keeps track of the current time of the system by a **global variable, curr_slot** which equals the current time in slots. . .
>
> A basic scheduling algorithm of cell/frame scheduler 102 scans forward in the timing wheel 400 with a limited look ahead, L, from the current time curr_slot. If it finds a first connection, say connection (i) with an LCD enqueued on the timing wheel (TW) within that range, i.e., (qslot(i) - curr_slot) < L, then cell/frame scheduler 102: a) sends out this cell or frame; b) **increments the curr_slot**; and c) computes the next time that this LCD has to be enqueued on the timing wheel 400 or 402.

Thus, the relied-upon portion of Delp fails to teach or suggest the limitation of claim 1 directed to moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table. Delp thus fails to remedy the fundamental deficiencies of Nguyen so as to reach the limitations of claim 1.

Accordingly, the proposed combination of Delp and Nguyen fails to teach or suggest at least the limitations of claim 1.

Moreover, the Examiner contends on page 5, first paragraph, of the present Office Action that "it would have been obvious to one skilled in the art to move an entry from one location to another, for the purpose of moving an entry to empty time slot and subsequently transmitting data associated with that entry." Applicants respectfully submit that this statement is a conclusory statement of the sort ruled insufficient by both the Federal Circuit and the U.S.

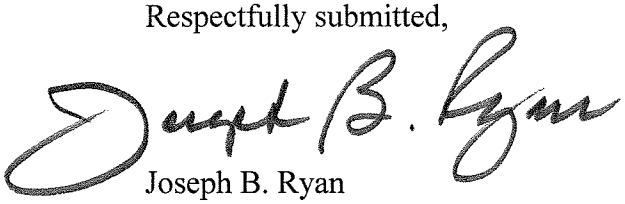
Supreme Court. See *KSR v. Teleflex*, 127 S.Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (U.S., Apr. 30, 2007), quoting *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

Independent claims 21 and 22 include limitations similar to those of independent claim 1 are thus believed allowable for at least the reasons identified above with regard to claim 1.

Dependent claims 2-10 and 18-20 are believed allowable for at least the reasons identified above with regard to claim 1.

In view of the foregoing, Appellants believe that claims 1-10 and 18-22 are in condition for allowance, and respectfully request the withdrawal of the present §103(a) rejection.

Respectfully submitted,



Date: April 7, 2008

Joseph B. Ryan
Attorney for Appellant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

CLAIMS APPENDIX

1. A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements; and

traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements;

wherein the scheduling circuitry is configured for utilization of at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot and being configured to store at least one entry, the scheduling circuitry being operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

2. The processor of claim 1 wherein the time slot table is stored at least in part in an internal memory of the processor.

3. The processor of claim 1 wherein the time slot table is stored at least in part in an external memory coupled to the processor.

4. The processor of claim 1 wherein a given one of the locations in the time slot table stores an identifier of one of the transmission elements that has requested transmission of a block of data in the corresponding time slot.

5. The processor of claim 1 wherein one or more of the data blocks comprise data packets.

6. The processor of claim 1 wherein the established traffic shaping requirement is substantially maintained by linking together identifiers of transmission elements generating requests that collide for a given time slot, from a single entry in the corresponding table location, and then scheduling the requesting elements for transmission in the order in which they are linked.

7. The processor of claim 1 wherein the scheduling circuitry provides dynamic maintenance of the time slot table such that identifiers of requesting transmission elements are entered into the table locations on a demand basis.

8. The processor of claim 1 wherein identifiers of the transmission elements comprise a structure for allowing a given one of the transmission element identifiers to be linked to another of the transmission element identifiers.

9. The processor of claim 8 wherein in the event of a collision between multiple transmission elements requesting a given one of the time slots, an identifier of a first one of the requesting transmission elements is entered into the corresponding location in the time slot table, and that identifier is linked to an identifier of a second of the requesting transmission elements, with similar linking between the identifier of the second requesting transmission element and an identifier of any subsequent one of the requesting transmission elements, a linked list of the multiple requesting elements thereby being created for the corresponding location in the time slot table.

10. The processor of claim 9 wherein upon transmission of a data block from one of the requesting transmission elements in the linked list of elements, a determination is made as to whether there are any further elements linked to that element, and if there are any further elements, the identifier of the next such element is determined and that identifier is written into the corresponding location in the time slot table.

18. The processor of claim 1 further comprising a transmit queue coupled to the scheduling circuitry and the traffic shaping circuitry, the transmit queue supplying time slot requests from transmission elements to the scheduling circuitry in accordance with the traffic shaping requirement established by the traffic shaping circuitry.

19. The processor of claim 1 wherein the processor comprises a network processor configured to provide an interface for data block transfer between a network and a switch fabric.

20. The processor of claim 1 wherein the processor is configured as an integrated circuit.

21. A method for use in a processor for scheduling data blocks for transmission from a plurality of transmission elements, the method comprising:

establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements; and

scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more transmission time slots, utilizing at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to one of the transmission time slots and being configured to store at least one entry, and further utilizing a linking of colliding transmission elements and movement of at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

22. A computer-readable medium comprising one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements, utilizing at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot and being configured to store at least one entry, wherein the one or more programs when executed implement the steps of:

establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements; and

scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more of the transmission time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None